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EXAMINER	
CHANG, SUNRAY	
ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/606,148	Applicant(s) TSUCHIYA ET AL.	
	Examiner Sunray Chang	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *Fig1,2,4,5* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2 - 3*. 2 sheets
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. *Claims 1 – 11 are presented for examination.*

2. *Claims 1 – 11 are rejected.*

Drawings

3. New corrected drawings are required in this application because "CONE" in figures have been misspelled as "CORN". Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "Logic Cone Unit" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

5. "Logic cone unit" has been frequently used in specification but is not shown in the figures:

(p3, L22) Comprising logic cone dividing unit for dividing a first circuit description defining the structure and specification of the circuit to be designed in "logic cone units", logic verification unit for verifying the logic by using the first circuit description and test vectors,

(p4, L8) A second feature of the present invention relates to a circuit designing method comprising a circuit description input step of entering a first circuit description defining the structure and specification of the circuit to be designed, a logic cone dividing step of dividing the first circuit description in "logic cone units",

(p5,L25;p6,L7;p6,L27;p11,L29) According to the circuit designing apparatus of the present invention, when the circuit description is changed in logic verification, changed points in the circuit description are automatically specified in "logic cone units", and plural test vectors are classified into those relating to the changed points and others not,

(p6,L1,20;p7,L3) Moreover, it is possible to analyze which part of the circuit is activated by a test vector, in the "logic cone unit", by every test vector, so that the test vectors can be managed and controlled strictly..

(p10,L10) The first circuit description is divided in "logic cone units" (logic cone dividing step, S102).

6. "Predetermined unit" has been frequently used in claims. Specification recites that "predetermined unit" is "logic cone" (p8, L7). But there is no recitation for the generation of "logic cone".

Claim Objections

7. Claim1 - 4, and 8 are objected to reject because of the following informalities: "and others not" is not a suitable description for separation between operations. More

detail descriptions are needed for avoiding confusion. Appropriate correction is required.

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

9. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

10. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

11. U.S. P/N No. 6,449,750 is issued to Tsuchiya on Sep. 10, 2002 hereafter referred to as Tsuchiya 1st.

12. Claim 1 – 11 rejected under the judicially created doctrine of double patenting over claim 1 – 27 of U.S. Patent No. 6,449,750 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

13. The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows:

14. Both design verification devices for semiconductor integrated circuits comprising specifying the changed points in the first portion of the device and classifying test vectors which inputted from user first based on the modifications between the circuits before and after the modification.

15. Both design verification devices with dividing unit, logic verification unit, recording unit, circuit changing processing, comparing results of circuits before and after alternation, specifying test vectors to modified circuits. Consider, for example, claim 4 of patented invention Tsuchiya 1st as compared to application claim 1. The only difference appears to be that the claim 1 of the patented invention Tsuchiya 1st recites more detail.

16. Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application that matured into a patent.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> *The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.*

17. Claims 1 - 11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

18. The phrase "predetermined unit" has been frequently used in claims and specification but has not been defined in the specification. The claims recite specifying the changed points of the circuit description automatically in "predetermined unit". Also The claims recite "circuits been designed in predetermined unit".

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

19. Claims 1 - 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

20. The phrase "predetermined unit" is ambiguous.

Claim Interpretation

21. The phrase, "Corn", is assumed to be "cone".

22. "Dividing Unit" in claim2, "Dividing" in claim4, "Dividing Process" in claim8 are recited but not showing in figures. In figure2, "Divide Logic Cone" is recited but is not recited in specification. It is assumed that "Dividing Unit" in claim2, "Dividing" in claim4, "Dividing Process" in claim8 are the same as "Divide Logic Cone" in figure2.

23. "Formal verification unit for verifying by formal technology using first and second circuit descriptions" does not clearly recite the function of the "formal verification unit". "Formal verification unit" is assumed to be regular verification.

24. "Logic cone" is not clearly recited. "Logic Cone" is assumed to be "structure and specification" of circuit based on "first circuit description defining the structure and specification of the circuit to be designed in logic cone units"(p3, L21).

25. "Logic cone unit" has been frequently used in specification without been clearly defined. "Logic cone unit" is assumed to be "logic cone dividing unit" (S102 Fig. 2; p10, L10).

26. "Predetermined unit" is frequently used in claims but does not clearly defined. Based on "the prepared circuit description is divided into predetermined units called 'logic cone' "(p8, L6-7). "Predetermined Unit" is assumed to be "logic cone".

27. The rejections behind are all based on these interpretations.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

28. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical

Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

29. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Kayhan Kucukcakar et al. (U.S. Patent No. 5,912,819 and Kucukcakar hereinafter).

30. Regarding Independent claim 1, Kucukcakar teaches unit for specifying the changed points (identifies the modified portion, Col 9, Line 62) of the circuit description (RTL implementation, Col 9, Line 63) automatically (automatically, Col 7, Line14) in predetermined unit (algorithmic description, Col 9, Line 49) and classifying (perform, Col 9, Line 64) the plural test vectors (design tasks, Col 9, Line 65) into those related with the changed points (modified portion, Col 9, Line 65) and others not (only, Col 9, Line 65).

31. Claims 2 – 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Douglas J. Gilbert et al. (U.S. Patent No. 5,805,861 and Gilbert hereinafter).

32. Regarding Independent Claims 2 and 8, Gilbert teaches dividing unit Stabilizing method, Col 4, Line 50) for dividing (partitioning, Col 4, Line 52) a first circuit description (previous circuit design version, Col 4, Line 52) defining the structure (net names, Col 4,

Line 50) and specification (components, Col 4, Line 50) of the circuit (previous circuit design version, Col 4, Line 52) to be designed in predetermined units (logic design, Col 4, Line 54); logic verification unit for verifying (identical, Col 4, Line 60) the logic (logic design, Col 4, Line 60) by using first circuit description (previous circuit design version, Col 4, Line 61) and test vectors (base net, Col 4, Line 56); profile information generating unit for storing (stored, Col 4, Line 47) the information (description, Col 4, Line 47) about the predetermined unit (gate – level description, Col 4, Line 47) in the first circuit description (inputs, Col 4, Line 45) to be activated by the test vector (nets, Col 4, Line 40) during logic verification (Logic optimizer, Col 4, Line 49) in every test vector as profile information (Logic design, Col 4, Line 40); circuit changing unit for changing (changed, Col 4, Line 5) first circuit description (integrated circuit, Col 4, Line 5) and generating (operated, Col 4, Line 5) a second circuit description (current design iteration, Col 4, Line 6); formal verification unit for verifying (verified, Col 7, Line 9) by formal technology (desired specification, Col 7, Line 10) using first and second circuit descriptions (behavior, detailed description, Col 7, Line 10 – 12);

specifying unit for specifying (assigned, Col 5, Line 9) the changed predetermined unit (new components and new names, Col 5, Line 8) relating to the change (selected cones, Col 5, Line 9) in second circuit description (current circuit design version, Col 5, Line 2) on the basis of the result of formal verification (behavior, detailed description, Col 7, Line 10 – 12); and test vector classifying unit for classifying (selected, Col 5, Line 3) the test vectors (components, net names, Col 5, Line 2 – 3) into those activating the

changed predetermined unit (subsection of the selected cone, Col 5, Line 3) and others not (selected cone, Col 5, Line 3) by using profile information.

33. *Regarding Independent Claim 3, Gilbert teaches* specifying (assigned, Col 5, Line 9) the changed points (new components and net names, Col 5, Line 8) of the circuit description (circuit design, Col 5, Line 10) automatically (automation, Col 1, Line 9) in predetermined unit (logic design, Col, 5, Line 13); and classifying (selected, Col 5, Line 3) the plural test vectors (components, net names, Col 5, Line 2) into those related (selected Col 5, Line 9) with the changed points (cone of logic, Col 5, Line 9) and others not (selected Col 5, Line 9), wherein the second and subsequent logic verification processes (current circuit design description, Col 5, Line 7) are executed (transferred, Col 5, Line 7) by using only the test vectors (new components and net names, Col 5, Line 8) relating to the changed points (do not exist in the selected cone, Col 5, Line 11).

34. *Regarding Independent Claim 4, Gilbert teaches* entering a first circuit description (previous circuit design, Col 4, Line 52) defining the structure (net names, Col 4, Line 50) and specification (components, Col 4, Line 50) of the circuit to be designed; dividing (Partitioning, Col 4, Line 52) first circuit description in predetermined units (logic design, Col 4, Line 54); verifying (identical, Col 4, Line 62) the logic (logic, Col 4, Line 61) by using first circuit description (previous circuit design, Col 4, Line 61) and test vectors (components and net names, Col 4, Line 63); storing stored, Col 4, Line 47) the information about the predetermined unit (logic design, Col 4, Line 40) in

first circuit description (gate level description, Col 4, Line 46) to be activated (input, Col 4, Line 48) by the test vector (components and nets, Col 4, Line 44) during logic verification (identical, Col 4, Line 40) in every test vector as profile information(gate level description, Col 4, Line 46); changing (modified, Col 4, Line 67) first circuit description previous circuit design, Col 5, Line1) and generating (in going, Col 5, Line 1) a second circuit description current circuit design, Col 5, Line 2); verifying (verified, Col 7, Line 9) by formal technology (desired specification, Col 7, Line 10) using the first and second circuit descriptions (behavior and detail description, Col 7, Line 10 – 12); specifying (assigned, Col 5, Line 9) the changed predetermined unit (subsection of the selected cone of logic design, Col 5, Line 9) relating to the change in second circuit description (current circuit description, Col 5, Line 10) on the basis of the result of formal verification (detailed description, Col 7, Line 12); and classifying (selected, Col 5, Line 3) the test vectors (components and net names, Col 5, Line 2 – 3) into those activating the changed predetermined unit (subsection of the selected cone, Col 5, Line 3) and others not by using profile information Logic design, Col 5, Line 4).

35. *Regarding dependent Claims 5 and 9, Gilbert teaches* the logic verification (identical logical structure, Col 5, Line 5) of the second circuit description (current circuit design, Col 5, Line 7) is executed (transferred, Col 5, Line 7) by using preferentially the test vector (new components and net names, Col 5, Line 8) for activating (assigned, Col 5, Line 9) the changed predetermined unit (those does not exist in the selected cones, Col 5, Line 11).

36. *Regarding dependent Claims 6, 10 and 11, Gilbert teaches* issuing conversion process, Col 7, Line 13) a circuit description (detailed description, Col 7, Line 14) and processing (complete, Col 7, Line 20) circuit manufacture (layout, Col 7, Line 22) by using circuit description (detailed description, Col 7, Line 18).

37. *Regarding dependent Claim 7, Gilbert teaches* issuing (conversion process, Col 7, Line 13) a circuit description (detailed description, Col 7, Line 14) and processing circuit design (remaining design processes, Col 7, Line 17) and manufacture (layout, Col 7, Line 22) by using circuit description (detailed description, Col 7, Line 14).

38. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tokunoh et al. (U.S. Patent No. 5,892,678) discloses input unit, storage unit, selecting unit, decision unit, process unit, component entry unit, verification unit, circuit changing unit. Carpenter et al. (U.S. Patent No. 5,862,149) discloses identify fault present, circuit node, test vector, test pattern, cones of logic, logic design, automatically generating test patterns, verify, storage. Tsuchiya et al. (U.S. Patent No. 6,449,750) discloses test vector classification, logic verification, formal verification, circuit changing, specifying unit, storing, dividing. Johannsen et al. (U.S. Patent No. 5,910,898) discloses circuit design tool, verify, logic equation, logical behavior.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sunray Chang whose telephone number is 703-305-8744. The examiner can normally be reached on M-F 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703-305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-746-3506.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-6833.

Sunray Chang
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December 31, 2003

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